AMENDMENTS TO THE CLAIMS

1. (CURRENTLY AMENDED) A method for generating a modified view of a circuit layout comprising the steps of:

receiving ~~said~~ circuit layout data from a design rule clean database;

extracting ~~a~~ base wafer layout data from said circuit layout data according to a set of computer executable instructions; and

modifying said base wafer layout data by combining one or more unused diffused blocks to form a single paveover cell according to said set of computer executable instructions.

2. (CURRENTLY AMENDED) The method according to claim 1, wherein the step of extracting said base wafer layout data further comprises:

extracting data for base layers of said one or more unused diffused blocks from said circuit layout data.

3. (CURRENTLY AMENDED) The method according to claim 2, wherein the step of extracting said base wafer layout data further comprises:

extracting layer tags from said circuit layout data.

4. (CURRENTLY AMENDED) The method according to claim 3, wherein the step of modifying said base wafer layout data further comprises:

removing metal in the extracted base layers of said one or more unused diffused blocks; and

combining the extracted base layers of said one or more unused diffused blocks with said metal removed into ~~a~~ said paveover cell.

5. (ORIGINAL) The method according to claim 4, further comprising:

flattening said paveover cell.

6. (CURRENTLY AMENDED) The method according to claim 1, further comprising the step of:

comparing one or more base layers of ~~said~~ the modified base wafer layout data with corresponding base layers of said circuit layout data.

7. (CURRENTLY AMENDED) The method according to claim ~~1~~2, further comprising:

placing an insulating layer over said base layers of said one or more unused diffused blocks; and

placing routing over ~~said~~ the insulated base ~~wafer~~ layers of said one or more unused diffused blocks, wherein said routing uses routing resources of said one or more unused diffused blocks.

8. (CURRENTLY AMENDED) The method according to claim 2, further comprising:

extracting data for one or more control layers of said one or more diffused blocks.

9. (CURRENTLY AMENDED) The method according to claim 8, wherein said data for said one or more control layers are extracted based upon any of (i) a clean design rule check (DRC), (ii) a clean layout versus schematic (LVS) check and (iii) both a clean DRC and a clean LVS check.

10. (CURRENTLY AMENDED) The method according to claim 2, wherein said one or more unused diffused blocks comprise one or more blocks selected from the group consisting of a hard macro, coreware, a standard cell and a memory.

11. (CURRENTLY AMENDED) The method according to claim ~~2~~1, further comprising the steps of:

generating a modified view of said circuit layout including said paveover cell; and

generating a second design rule clean database comprising said modified view of said circuit layout, wherein said second database is used for subsequent steps of a design when one or more diffused blocks of said circuit layout are unused in said design.

12. (CURRENTLY AMENDED) A design tool for automating a process for generating a modified view of a circuit layout comprising:

means for extracting data for base layers of one or more diffused blocks of said circuit layout from a first design rule clean database; ~~and~~

means for forming a paveover cell comprising the extracted base layers, wherein said design tool ~~facilities~~ facilitates reuse ~~or~~ of routing resources of said one or more diffused blocks; and

means for generating a second design rule clean database containing said modified view of said circuit layout, wherein said modified view includes said paveover cell.

13. (CURRENTLY AMENDED) A design tool for automating a process for generating a modified view of a circuit layout comprising:

a first set of computer executable instructions configured to extract data for base layers of one or more unused diffused blocks of a circuit layout from a first database;

a second set of computer executable instructions configured to generate a paveover cell comprising ~~said~~ the extracted base layers of said one or more unused diffused blocks; and

a third set of computer executable instructions configured to generate a second database comprising said paveover cell, wherein routing resources of said one or more unused diffused blocks are available for ~~reuse~~ use by other circuitry of said circuit layout.

14. (CURRENTLY AMENDED) The design tool according to claim 13, wherein:

said first set of computer executable instructions and said second set of computer executable instructions comprise a run deck configured to control a commercially available tool suite.

15. (ORIGINAL) The design tool according to claim 13, wherein:

said first set of computer executable instructions and said second set of computer executable instructions are stored in a computer readable media.

16. (CURRENTLY AMENDED) The design tool according to claim 13, further comprising:

a fourth set of computer executable instructions configured to perform one or more operations selected from the group consisting of inserting metal utilization information (mu), creating route guides, avoiding crosstalk and avoiding slew errors.

17. (CURRENTLY AMENDED) The design tool according to claim 13, wherein said design tool is further ~~comprising the step of:~~

~~generating~~ configured to generate a netlist in response to a layout versus schematic (LVS) verification operation on said paveover cell.

18. (CURRENTLY AMENDED) The design tool according to claim 13, wherein:

said third set of computer executable instructions are further configured to generate said second database ~~according to~~ using a metal utilization (mu) annotation file generated in response to a design rule checking (DRC) operation.

19. (ORIGINAL) The design tool according to claim 13, wherein said design tool is configured to present one or more frame views of said paveover cell.

20. (ORIGINAL) The design tool according to claim 13, further comprising:

a fourth set of computer executable instructions configured to (i) compare one or more base layers of said paveover cell to corresponding base layers of said circuit layout and (ii) assure said base layers of said paveover cell correctly compare with said corresponding base layers of said circuit layout.